ABSTRACT

A method of characterizing gate leakage current in the fabrication of integrated circuits is described. A MOSFET model is provided including a gate electrode deposed over a gate oxide layer on a substrate and source and drain regions associated with the gate electrode. Device current is measured at four terminals simultaneously wherein one of the terminals is a drain terminal. The other terminals are the source, gate, and substrate. The portion of the device current measured at the drain terminal that is contributed by gate current is evaluated. The evaluated gate current contribution is subtracted from the drain terminal current measurement to obtain pure drain current. Fitting procedures are performed to obtain curves for the device currents. The pure drain current is used to extract mobility model parameters.